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Chipkarte

Carte à circuit intégré

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Description

The present invention relates to an IC card and, more particularly, to an IC card which has, in addition to a semiconductor memory for storing the main data, a semiconductor memory for storing physical information concerning the card and format information concerning the data in the card.

DESCRIPTION OF THE RELATED ART:

Fig. 4 shows an IC card of the type described above. The IC card has a 256 K bit static RAM 1 serving as an area for storing main data, and a 64 K bit EEPROM 2 which is adapted to store physical information concerning the IC card, e.g., type and capacity of the memory, access time and so on, as well as format information concerning the data stored in the IC card. A mode control circuit 3 is connected to the static RAM 1 and the EEPROM 2. In addition, all the address signal lines A_0 to A_{14} of an address BUS 5 are connected to the static RAM 1. Selected address signal lines A_0 to A_{12} of the BUS are also connected to the EEPROM 2. Furthermore, a data BUS 7 including 8-bit data signal lines D_0 to D_7 is connected to the static RAM 1 and also to the EEPROM 2.

The mode control circuit 3 receives a card enable signal $\overline{CE}$ and a memory selection signal $\overline{REG}$. A chip enable signal S_1 of "L" level is delivered to the static RAM 1 when the card enable signal $\overline{CE}$ is "L" while the memory selection signal $\overline{REG}$ is of "H" level. When both the card enable signal $\overline{CE}$ and the memory selection signal $\overline{REG}$ are of "L" level, a chip enable signal S_2 of "L" level is delivered to the EEPROM 2.

The operation of this IC card is as follows. When it is desired to use the static RAM 1, a terminal device which is not shown sets the card enable signal $\overline{CE}$ to "L" level and sets the memory selection signal $\overline{REG}$ to "H" level. As a result, a chip enable signal S_1 of "L" level is delivered from the mode control circuit 3 to the static RAM 1 so that the static RAM 1 becomes ready to operate. In this state, an address is appointed through the address signal lines A_0 to A_{14}, and read control signal $\overline{OE}$ and write control signal $\overline{WE}$ are respectively set to "L" and "H" levels, so that data stored in the appointed address of the RAM 1 appears on the data BUS 7. Conversely, when the read control signal $\overline{OE}$ and the write control signal $\overline{WE}$ are respectively set to "H" and "L" levels, data on the data BUS 7 are written in the appointed address of the static RAM 1. The data in the static RAM 1 is extinguished when the power supply is turned off.

On the other hand, when the EEPROM 2 is to be used, both the card enable signal $\overline{CE}$ and the memory selection signal $\overline{REG}$ are set to "L" levels. As a result, a chip enable signal S_2 of "L" level is delivered to the EEPROM 2 from the mode control circuit 3, thereby enabling the EEPROM 2 to operate. Reading and writing of data are conducted in the same manner as those in the case of the static RAM 1. The data in the EEPROM 2 is not extinguished even when the power supply is turned off.

When both the static RAM 1 and the EEPROM 2 are not to be used, the card enable signal $\overline{CE}$ is set to "H" level. In this case, both the chip enable signals S_1 and S_2 are set to "H" so that the static RAM 1 and the EEPROM 2 become inoperative.

In this known IC card, the EEPROM 2 can be accessed easily through a terminal device (not shown) as described above, so that a problem has been encountered that the physical information concerning the card stored in the EEPROM 2 may be rewritten accidentally or willfully.

Generally, unauthorised memory access can be prevented by hardware and/or software control means inhibiting access to a given range of addresses in the memory, cf. e.g. EP-A-0 331 407 disclosing an inhibition address checker.

SUMMARY OF THE INVENTION

Accordingly, an object of the present invention is to provide an IC card which prevents physical information stored therein from being easily rewritten through a terminal device.

To this end, according to the present invention, there is provided an IC card comprising:

a first semiconductor memory for storing data;
a second semiconductor memory for storing physical information concerning the IC card;
a control circuit for selectively enabling one of said first and second semiconductor memories to operate, said second semiconductor memory being non-volatile;
an address BUS connected to said first and second semiconductor memories; and
a data BUS connected to said first and second semiconductor memories; characterised by
a decoder for decoding a write control signal for said second semiconductor memory using part of the address signal necessary for making access to said second semiconductor memory and delivering the decoded write control signal to said second semiconductor memory;
wherein said address BUS has a plurality of signal lines corresponding to a plurality of bits, said decoder is operative for selectively decoding said write control signal for said second semiconductor memory in accordance with the levels of at least one of said plurality of signal lines whereby said second semiconductor memory has a rewritable memory region and a non-rewritable memory region.

In the present invention, the decoder decodes the write control signal for the second semiconductor memory by using part of the address signal which is necessary for making access to the second semiconductor memory, whereby a part of the second semiconductor

memory is changed into a non-writable area.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a block diagram of an IC card in accordance with an embodiment of the present invention;

Fig. 2 is an illustration of the operation of a decoder 4 incorporated in the embodiment shown in Fig. 1;

Fig. 3 is an illustration showing an arrangement of memories in EEPROM; and

Fig. 4 is a block diagram of a conventional IC card.

DESCRIPTION OF THE PREFERRED EMBODIMENT

A preferred embodiment of the present invention will be described with reference to the accompanying drawings.

Referring to Fig. 1, an IC card embodying the present invention has a 256 K bits static RAM 1 which provides an area for storing main data, and a 64 K bits EEPROM 2 adapted for storing physical information concerning the IC card, e.g., type and capacity of the memory, access time and so on, as well as format information concerning data stored in the IC card. A mode control circuit 3 is connected both to the static RAM 1 and the EEPROM 2. All the address signal lines A_0 to A_{14} of an address BUS 5 are connected to the static RAM 1, and selected address lines A_0 to A_{12} are also connected to the EEPROM 2. A data BUS 7 formed of 8-bit signal lines D_0 to D_7 is connected both to the static RAM 1 and the EEPROM 2.

The mode control circuit 3 receives a card enable signal $\overline{CE}$ and a memory selection signal REG. When the card enable signal $\overline{CE}$ is of "L" level while the memory selection signal $\overline{REG}$ is of "H" level, the mode control circuit 3 delivers a chip enable signal S_1 of "L" level to the static RAM 1, whereas, when both the card enable signal $\overline{CE}$ and the memory selection signal $\overline{REG}$ are of "L" level, the mode control circuit 3 delivers a chip enable signal S_2 of "L" level to the EEPROM 2.

A decoder 4 is connected to a write control input terminal 2a of the EEPROM 2. Two signal lines A_{11} and A_{12} out of the address BUS 5 are connected to the decoder 4. The decoder 4 decodes a write control signal $\overline{WE}$ in accordance with the levels of the signal lines A_{11} and A_{12}, and delivers to the EEPROM 2 a new write control signal WED shown in Fig. 2. More specifically, when both the signal lines A_{11} and A_{12} are of "L" level, the decoder 4 decodes the write control signal $\overline{WE}$ of "L" level to a write control signal WED of "H" level, thereby prohibiting writing in the EEPROM 2.

The write control signal $\overline{WE}$ is directly supplied to a write control input terminal 1a of the static RAM 1. A read control signal $\overline{OE}$ is input both to the read control signal input terminals 1b and 2b of the static RAM 1 and the EEPROM 2.

In the described embodiment, the static RAM 1 serves as the first semiconductor memory, while the EEPROM 2 serves as the second semiconductor memory.

The operation of this embodiment is as follows.

When it is desired to use the static RAM 1, a terminal device (not shown) sets the card enable signal $\overline{CE}$ to "L" level, while setting the memory selection signal $\overline{REG}$ to "H" level. Consequently, the mode control circuit 3 delivers a chip enable signal S_1 of "L" level to the static RAM 1, thus enabling the static RAM 1 to operate. In this state, when the desired address is appointed through the address signal lines A_0 to A_{14} of the address BUS 5, while the read control signal $\overline{OE}$ and the write control signal $\overline{WE}$ are respectively set to "L" and "H" levels, the data in the appointed address of the static RAM 1 appears on the data BUS 7. Conversely, when the read control signal $\overline{OE}$ and the write control signal $\overline{WE}$ are respectively set to "H" and "L" levels, the data on the data BUS 7 are written in the appointed address of the static RAM 1. The data in the static RAM 1 is extinguished when the power is turned off.

On the other hand, when the EEPROM 2 is to be used, both the card enable signal $\overline{CE}$ and the memory selection signal $\overline{REG}$ are set to "L" level. Consequently, a chip enable signal S_2 of "L" level is delivered from the mode control circuit 3 to the EEPROM 2, thus enabling the EEPROM 2 to operate.

The operation for reading data from the EEPROM 2 is conducted in the same manner as that in the case of the static RAM 1. Namely, the data stored in the address of the EEPROM 2 appointed through the address signal lines A_0 to A_{12} of the address BUS 5 appears on the data BUS 7 when the read control signal $\overline{OE}$ and the write control signal $\overline{WE}$ are respectively set to "L" and "H".

For writing data in the EEPROM 2, the address in which the data is to be written is appointed through the address signal lines A_0 to A_{12} of the address BUS 5, and the read control signal $\overline{OE}$ and the write control signal $\overline{WE}$ are respectively set to "H" and "L" levels. The write control signal $\overline{WE}$ is input to the decoder 4 so as to be decoded in accordance with the levels of the signal lines A_{11} and A_{12} connected to the decoder 4. As will be seen from Fig. 2, in the cases other than the case where both the signal lines A_{11} and A_{12} are of "L" level, i.e., when one of the addresses 800 to 1FFF by hexadecimal notation has been appointed, the write control signal $\overline{WE}$ of "L" level is input to the EEPROM 2 as a new write control signal WED while maintaining the level "L". Consequently, the data on the data BUS 7 is written in the appointed address of the EEPROM 2. Conversely, when both the signal lines A_{11} and A_{12} are of "L" level, i.e., when one of addresses 0 to 7FF by hexadecimal notation has been appointed, the write control signal $\overline{WE}$ of the "L" level is decoded into a new write control signal WED of "H" level, and this new write control signal WED is input to the EEPROM 2, so that the writing of data in the EEPROM 2 is prohibited.

Thus, in the described embodiment, as shown in Fig. 3, the area of the addresses 0 to 7FF of the EEPROM 2

forms a non-rewritable region R1, while the area of addresses 800 to 1FFF forms a rewritable region R2. Therefore, the physical information concerning the IC card, which should not be rewritten easily, is stored in this non-rewritable region R1, while other information such as format information of the data is stored in the rewritable region R2. The physical information concerning the card, stored in the memory region R1, cannot easily be rewritten through the terminal device. The data in the EEPROM 2 is not extinguished even when the power is turned off.

When both the static RAM 1 and EEPROM 2 are not to be used, the card enable signal $\overline{CE}$ input to the mode control circuit 3 is set to "H" level. In this case, the chip enable signals S_1 and S_2 are set to "H" level regardless of the level of the memory selection signal $\overline{REG}$, so that both the static RAM 1 and the EEPROM 2 become inoperative.

Although a 256 K bit static RAM 1 is used as the first semiconductor memory in the described embodiment, this is not exclusive and semiconductor memories of different types and capacities can be used equally well. It is also to be understood that the 64 K bit EEPROM 2 can be substituted by other suitable writable semiconductor memory. The described decoding method performed by the decoder 4 also is illustrative and the same effect can be obtained also when other decoding methods are used.

As will be understood from the foregoing description, in the IC card of the present invention, the physical information concerning the IC card is not easily rewritable through a terminal device, so that the reliability of the IC card can be greatly improved.

Claims

1. An IC to card comprising:

   a first semiconductor memory (1) for storing data;
   a second semiconductor memory (2) for storing physical information concerning the IC card;
   a control circuit (3) for selectively enabling one of said first and second semiconductor memories to operate, said second semiconductor memory being non-volatile;
   an address BUS (5) connected to said first and second semiconductor memories; and
   a data BUS (7) connected to said first and second semiconductor memories;
   characterised by
   a decoder (4) for decoding a write control signal ($\overline{WE}$) for said second semiconductor memory using only a part of the address signal necessary for making access to said second semiconductor memory and delivering the decoded write control signal (WED) to said second semiconductor memory;
   wherein said address BUS (5) has a plurality of signal lines (A0 ~ A14) corresponding to a plurality of bits, said decoder (4) is operative for selectively decoding said write control signal ($\overline{WE}$) for said second semiconductor memory (2) in accordance with the levels of at least one of said plurality of signal lines whereby said second semiconductor memory has a rewritable memory region (R2) and a non-rewritable memory region (R1).

2. An IC card according to claim 1, wherein said non-rewritable memory region stores said physical information concerning the IC card.

3. An IC card according to claim 1, wherein said second semiconductor memory has a PROM.

Patentansprüche

1. IC-Karte, die folgendes aufweist:

   - einen ersten Halbleiterspeicher (1), um Daten zu speichern,
   - einen zweiten Halbleiterspeicher (2), um physikalische Informationen zu speichern, welche die IC-Karte betreffen,
   - eine Steuerschaltung (3), um selektiv einen der ersten und zweiten Halbleiterspeicher zum Betrieb freizugeben, wobei der zweite Halbleiterspeicher nicht-flüchtig ist,
   - einen Adreßbus (5), der mit dem ersten und dem zweiten Halbleiterspeicher verbunden ist, und
   - einen Datenbus (7), der mit dem ersten und dem zweiten Halbleiterspeichern verbunden ist,

   gekennzeichnet durch
   einen Dekodierer (4), um ein Schreib-Steuersignal ($\overline{WE}$) für den zweiten Halbleiterspeicher zu dekodieren, wobei der Dekodierer (4) nur einen Teil des Adreßsignals verwendet, das notwendig ist, um auf den zweiten Halbleiterspeicher zuzugreifen, und das dekodierte Schreib-Steuersignal (WED) an den zweiten Halbleiterspeicher liefert,
   wobei der Adreßbus (5) eine Vielzahl von Signalleitungen (A0 - A14) entsprechend einer Vielzahl von Bits aufweist und der Dekodierer (4) so arbeitet, daß er das Schreib-Steuersignal ($\overline{WE}$) für den zweiten Halbleiterspeicher (2) gemäß den Pegeln von zumindest einer der Vielzahl von Signalleitungen selektiv dekodiert, wobei der zweite Halbleiterspeicher einen überschreibbaren Speicherbereich (R2) und einen nicht-überschreibbaren Speicherbereich (R1) aufweist.

2. IC-Karte nach Anspruch 1, dadurch gekennzeichnet, daß der nicht-überschreibbare Speicherbereich die physikalischen Informationen speichert, welche die IC-Karte betreffen.

3. IC-Karte nach Anspruch 1, dadurch gekennzeichnet, daß der zweite Halbleiterspeicher einen PROM aufweist.

Revendications

1. Carte à circuit intégré comprenant :

une première mémoire à semi-conducteur (1) pour mémoriser une donnée;
une seconde mémoire à semi-conducteur (2) pour mémoriser une information physique concernant la carte à circuit intégré;
un circuit de contrôle (3) pour sélectivement permettre à l'une desdites première et seconde mémoires à semi-conducteur de fonctionner, ladite seconde mémoire à semi-conducteur étant non volatile;
un BUS adresses (5) relié auxdites première et seconde mémoires à semi-conducteur; et
un BUS de données (7) relié auxdites première et seconde mémoires à semi-conducteur;
caractérisé par
un décodeur (4) pour décoder un signal de commande d'écriture ($\overline{WE}$) pour ladite seconde mémoire à semi-conducteur utilisant seulement une partie du signal d'adresse nécessaire pour effectuer l'accès à ladite seconde mémoire à semi-conducteur et fournir le signal de commande d'écriture décodé (WED) à ladite seconde mémoire à semi-conducteur;
où ledit BUS d'adresses (5) comporte un certain nombre de lignes de signaux (A0~A14) correspondant à un certain nombre de bits, ledit décodeur (4) peut fonctionner pour sélectivement décoder ledit signal de commande d'écriture ($\overline{WE}$) pour ladite seconde mémoire à semi-conducteur (2) selon les niveaux d'au moins l'une de ladite pluralité de lignes de signaux, de la sorte ladite seconde mémoire à semi-conducteur a une région de mémoire réinscriptible (R2) et une région de mémoire non réinscriptible (R1).

2. Carte à circuit intégré selon la revendication 1, dans laquelle la région de mémoire non réinscriptible précitée mémorise l'information physique précitée concernant la carte à circuit intégré.

3. Carte à circuit intégré selon la revendication 1, dans laquelle la seconde mémoire à semi-conducteur précitée a une PROM.

FIG. 1

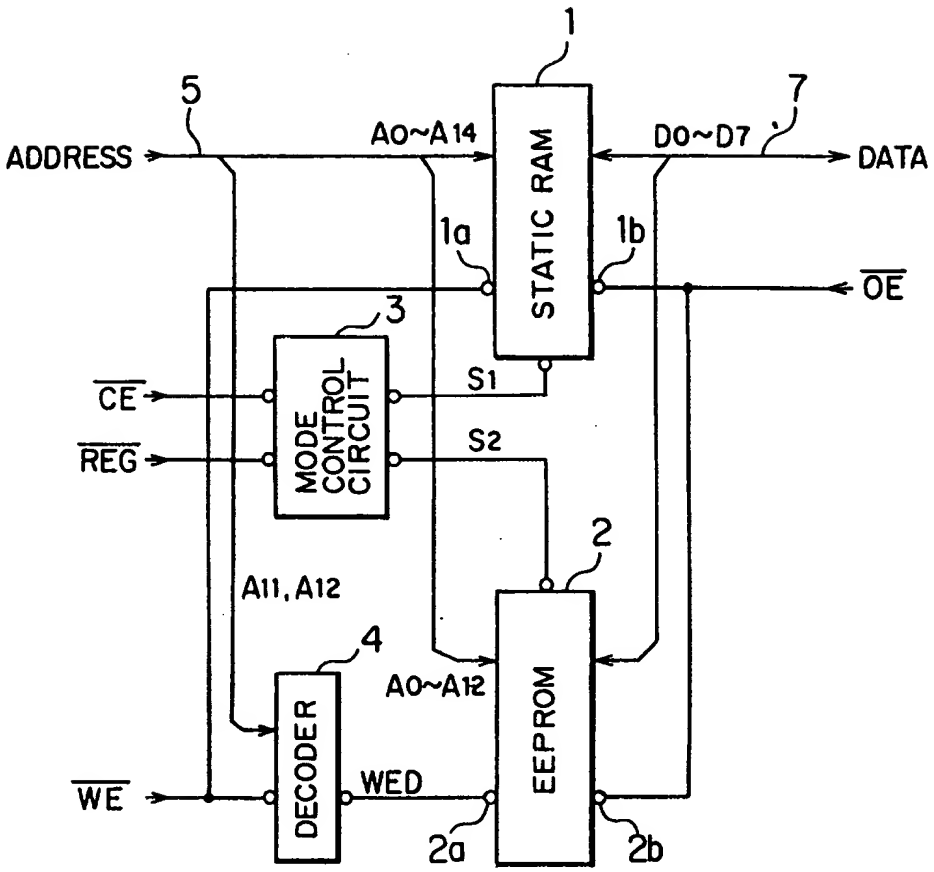
1
5
7
ADDRESS
A0~A14
D0~D7
DATA
STATIC RAM
1a
1b
OE
3
CE
REG
MODE CONTROL CIRCUIT
S1
S2
2
A11, A12
4
A0~A12
EEPROM
DECODER
WE
WED
2a
2b

FIG. 2

A11	A12	WE	WED
X	X	H	H
L	L	L	H
H	L	L	L
L	H	L	L
H	H	L	L

FIG. 3

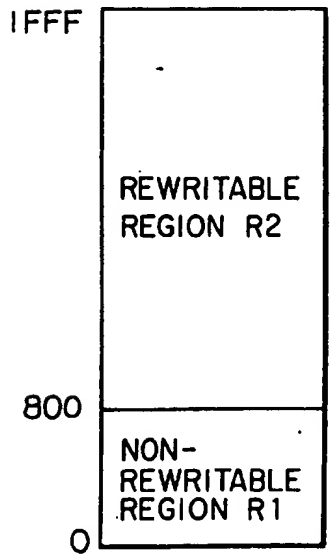

FIG. 4
PRIOR ART